WHAT IS CLAIMED IS:

1. A method of checking the resistance of a programmable element in an integrated circuit, comprising the steps of:

producing a first voltage at a first node based on the resistance of a programmable element;

producing a second voltage at a second node based on a known resistance; and

comparing said first and second voltages and producing an output signal in response to said comparison, the binary value of said output signal indicating whether the resistance of the programmable element is higher or lower than the known resistance.

2. The method of claim 1, wherein it further comprises:

equilibrating said voltages at said first and second nodes; and

performing said step comparing said first and second voltages after sufficient time has elapsed to allow said first and second voltages to change, respectively, based on the known resistance and the resistance of said programmable element.

3. The method of claim 2, wherein the voltages at the first and second nodes are equilibrated at the same approximate voltage between V_{CC} and zero volts.

4. A method of checking the resistance of a programmable element in an integrated circuit comprising:

providing a first node at which a first voltage is produced based on the resistance of a programmable element;

providing a second node at which a second voltage is produced based on a known resistance;

equilibrating the voltages at the first and second nodes; and

comparing the voltages at the first and second nodes and producing an output signal in response to said comparison, the binary value of said output signal indicating whether the resistance of the programmable element is higher or lower than the known resistance.

5. Apparatus for checking the resistance of programmable elements in an integrated circuit, comprising:

circuitry defining a programmable circuit, said circuitry including a programmable element having a resistance and said circuitry including a first node at which a voltage may be developed that is based on the resistance of the programmable element;

circuitry for producing a reference voltage at a second node, the reference voltage being based on the value of a known resistance; and

circuitry which compares the voltage on the first node to the reference voltage on the second node and which produces an output signal whose binary value indicates whether the value of the resistance of the programmable element is higher or lower than the value of the known resistance.

6. The apparatus of claim 5, comprising circuitry for equilibrating the voltages at the first and second nodes.

7. The apparatus of claim 5, wherein the programmable element comprises an antifuse element.

8. The apparatus of claim 5, wherein the programmable element comprises an ovonic element.

9. In an integrated circuit, apparatus comprising:

a plurality of programmable circuits, each programmable circuit including a programmable element having a resistance and a first node at which a voltage may be developed that is based on the resistance of the programmable element, the first nodes of all said programmable circuits being joined in a common connection;

selection circuitry for selecting one of said programmable circuits;

circuitry for producing a reference voltage at a second node, the reference voltage being based on the value of a known resistance; and

circuitry which compares said voltage at the first node of the selected programmable circuit to the reference voltage at the second node and which produces an output signal whose binary value indicates whether the value of the resistance of the programmable element in the selected programmable circuit is higher or lower than the value of the known resistance.

10. The apparatus of claim 9, comprising circuitry for equilibrating the voltages at the first and second nodes.

11. The apparatus of claim 9, comprising circuitry for varying the value of the known resistance.

12. The apparatus of claim 9, wherein said circuitry which compares the voltage at the first node of the selected bit of antifuse to the reference voltage at the second node comprises a comparator.

13. The apparatus of claim 9, wherein the programmable element comprises an antifuse element.

14. The apparatus of claim 9, wherein the programmable element comprises an ovonic element.

15. An apparatus for checking the resistance of a programmable element in an integrated circuit, comprising:

means for producing a first voltage at a first node based on a known resistance;

means for producing a second voltage at a second node based on the resistance of a programmable element; and

means for comparing the first voltage to the second voltage and producing an output signal in response to said comparison, the binary value of said output signal indicating whether the resistance of the programmable element is higher or lower than the known resistance.

16. The apparatus of claim 15, comprising:

means for equilibrating the voltages at the first and second nodes.

17. The apparatus of claim 15, wherein the programmable element comprises an antifuse element.

18. The apparatus of claim 15, wherein the programmable element comprises an ovonic element.

19. An integrated circuit, comprising:

a plurality of programmable circuits, each programmable circuit including a programmable element having a resistance and a first node at which a voltage may be developed that is based on the resistance of the programmable element, the first nodes of all programmable circuits being joined in a common connection;

a decoder for decoding a first address signal and sending a first enabling signal to each of said plurality of programmable circuits;

a reference circuit for producing a reference voltage at a second node, the reference voltage being based on the value of a known resistance; and

a comparator circuit which compares the voltage at the first node of the selected programmable circuit to the reference voltage at the second node and which produces an output signal whose binary value indicates whether the value of the resistance of the programmable element in the selected programmable circuit is higher or lower than the value of the known resistance.

20. The integrated circuit of claim 19, wherein each of said plurality of programmable circuits comprises:

means for receiving said first enabling signal connected to said programmable element;

means for receiving said first address signal connected to said programmable element;

means for transmitting said voltage to said first node; and

first means for receiving a second enabling signal, said means for transmitting said voltage to said first node being operable to transmit said voltage when means for receiving said first enabling signal receives said first enabling signal and said means for receiving said first address signal receives said first address signal and said first means for receiving said second enabling signal receives said second enabling signal.

21. The integrated circuit of claim 20, wherein said reference circuit comprises:

second means for receiving said second enabling signal;

means for initially equilibrating said voltage at said first node with said reference voltage; and

means for receiving an equilibrate signal that enables said means for initially equilibrating said voltage at said first node with said reference voltage;

said means for initially equilibrating said voltage at said first node with said reference voltage being operable to initially equilibrate said voltage at said first node with said reference voltage when said second means for receiving said second enabling signal receives said second enabling signal and said means for receiving an equilibrate signal that enables said means for initially equilibrating said voltage at said first node with said reference voltage receives said signal that enables said means for initially equilibrating said voltage at said first node with said reference voltage.

22. The apparatus of claim 20, wherein the said programmable element comprises an antifuse element.

23. The apparatus of claim 20, wherein the programmable element comprises an ovonic element.

24. A semiconductor memory device, comprising:

a memory array;

a plurality of programmable circuits, each programmable circuit including a programmable element having a resistance and a first node at which a voltage may be developed that is based on the resistance of the programmable element, the first nodes of all programmable circuits being joined in a common connection;

means for producing a first voltage at a first node based on a known resistance;

means for producing a second voltage at a second node based on the resistance of a programmable element; and

means for comparing the first voltage to the second voltage and producing an output signal in response to said comparison, the binary value of said output signal indicating whether the resistance of the programmable element is higher or lower than the known resistance.

25. The apparatus of claim 24, comprising:

means for equilibrating the voltages at the first and second nodes.

26. The apparatus of claim 24, wherein the programmable element comprises an antifuse element.

27. The apparatus of claim 24, wherein the programmable element comprises an ovonic element.